REMARKS

Claims 1-3, 7, 16, 17, 19-23, and 33-36 are pending. Claims 1 and 16 have been amended, claims 3 and 22 have been cancelled, and new claims 27 and 38 are added with this response. Reconsideration of the application is respectfully requested for at least the following reasons.

I. REJECTION OF CLAIMS 1-3, 7, AND 33-34 UNDER 35 U.S.C. § 103(a).

Claims 1-3, 7, and 33-34 were rejected under §103(a) as obvious over U.S. Pat. No. 6,545,358 (Jeong) in view of U.S. Pat. No. 5,117,276 (Thomas). Withdrawal of this rejection is requested for at least the following reasons.

As amended, claim 1 of the present invention relates to an integrated circuit, comprising a protective overcoat formed over the metallization layers, and having vias through it, wherein the protective overcoat comprises one or more layers selected from a group consisting of a silicon oxynitride layer, a silicon oxide layer, and a silicon nitride layer. The Office Action states that Jeong teaches a protective overcoat layer made of silicon oxide. (See, OA, p.3, lns. 14-15 and Joeng, col.4, lns. 60). However, it is respectfully noted that Jeong does not teach such a protective overcoat.

In the prior art section of the Jeong, an interlevel insulating layer 7 is taught. (*See, e.g.,* figure 1). In the detailed description section of the cited art, Jeong teaches an insulating layer 26 formed onto the first metal layer 23 and below the first plug 32. (*See, e.g.,* figure 6). This insulating layer is removed during processing through blanket etch (e.g., chemical mechanical polishing (CMP)) and then ***a subsequent, separate interlevel insulating layer 27*** (associated, by the Office Action, with the protective coating) is added to the substrate. (*See, e.g.,* figure 2; col. 5, lns. 11-15) ***Jeong teaches that the insulating layer 26 can be a silicon oxide layer, but fails to teach that the interlevel insulating layer 7 and 27, is a silicon oxide material.*** Jeong is silent as to the composition of the interlevel insulating layers 7 and 27.

Further, one skilled in the art would not necessarily use the material associated with the insulating layer 26 for the layers 7 and 27 (associated with a protective overcoat layer). One skilled in the art would recognize that ***a protective coating layer***

is different than other dielectric layers of an integrated chip as a protective overcoat is formed over the substrate of a semiconductor die prior to removal from the conventional silicon wafer processing equipment and commencement of metal plating for far back end of the line metallization. Therefore, the properties and materials required for a protective overcoat are not necessarily the same as those required for regular inter level dielectric (ILD) depositions. For example, ILD materials are often unique low-k materials employed to reduce capacitive crosstalk in signals of neighboring metallization lines. Accordingly, withdrawal of the rejection is respectfully requested.

Claims 2, 7, 33, and 34 depend upon independent claim 1 and add further limitations thereto. Because the primary reference does not teach the present invention of claim 1, claims 2, 7, 33, and 34 are not taught by the cited art. Accordingly, withdrawal of these rejections is also respectfully requested

II. REJECTION OF CLAIMS 16, 19-23, AND 36 UNDER 35 U.S.C. § 103(a).

Claims 16, 19-23, and 36 were rejected under §103(a) as being obvious over U.S. Pat. No. 6,545,358 (Jeong) in view of U.S. Pat. No. 6,218,282 (Buynoski). Withdrawal of this rejection is requested for at least the following reasons.

As amended, claim 16 relates to an integrated circuit, comprising a semiconductor substrate comprising one or more metallization layers having an uppermost layer comprising bond pads, and a protective overcoat formed over the metallization layers, and having vias through it, wherein multiple vias are formed over individual bond pads respectively, and wherein the protective overcoat comprising one or more layers selected from the group consisting of silicon oxynitride layers, silicon oxide layers and silicon nitride layers. Jeong fails to teach that the uppermost layer of the substrate comprises a bond pad, or that the protective overcoat consists of one or more of a silicon oxynitride layer, a silicon oxide layer, and a silicon nitride layer and Buynoski fails to remedy these deficiencies.

As admitted in the Office Action, Jeong does not teach multiple vias formed over individual bond pads. (*See,* OA dated 10/2/07, text just above the figure on page 4.).

Although it has been alleged that Buynoski (Fig. 4) cures this deficiency by showing an integrated circuit ***having multiple vias 1 formed over individual bond pads*** (metal 1), it is respectfully argued that Buynoski fails to teach an integrated circuit having multiple vias formed over individual bond pads. The Office Action states that Buynoski clearly shows an integrated circuit having multiple vias 1 formed over individual bond pads (metal 1). (*See*, p. 6, lns. 30-32). However, ***one skilled in the art would recognize that a metal 1 layer cannot be a bond pad in practical integrated chips designed for "high density... semiconductors devices comprising submicron dimensions"*** as taught by Buynoski. (*See, e.g.,* col. 1, lns. 17-19). In practical integrated chip design, low-k dielectric layers having a ***weak structural*** support are used on contact and thin (*i.e.,* low) metal levels to decrease capacitance and to decrease contact spacing, thereby decreasing time dependent dielectric breakdown (TDDB). These low-k dielectric layers do not provide the structural support necessary for bonding unless there is a via support structure below the metal to be bonded to. However, in practical integrated chip design the contacts below the metal 1 layer are organized in accordance with device layout considerations and therefore can not be laid out to provide the required density of via support for wire bonding on the first metal level.

Furthermore, Buynoski specifically states that the bonding pad area as element 41. (*See,* col. 5, lns. 65-66). One skilled in the art would recognize that the structures below element 41 (metal 1 – metal 5 and via 1 – via 5) are lower levels within the metal stack ***and are not part of the bond pad 41***. In particular, the dense via structure of Buynoski points to the fact that Buynoski intended these lower metal and via levels to be support levels to the bonding pad 41, not the bonding pad. (*See, e.g.,* figure 1). Therefore, ***Buynoski fails to teach a bond pad 41 that has multiple vias formed over it.*** Accordingly, for at least this additional reason, withdrawal of these rejections are respectfully requested.

Moreover, as stated above, ***Jeong fails to teach a protective overcoat formed of silicon silicon oxynitride layers, silicon oxide layers and silicon nitride layers*** as taught in claim 16 of the present invention.

Claims 17, 19-21, 23, and 36 depend upon claim 16, respectively, and add further limitations thereto. The primary reference does not teach or suggest the present invention of claim 16, and Buynoski fails to remedy the deficiencies in the primary reference. Therefore, claims 16-7, 19-21, 23, and 36 are also not taught by the cited art. Accordingly, withdrawal of these rejections are respectfully requested.

III. CONCLUSION

For at least the above reasons, pending claims currently under consideration are believed to be in condition for allowance and notice thereof is requested.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

In addition, should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 20-0668, TI-36853.

Respectfully submitted,
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